A 2-20 GHz DUAL CHANNEL RECEIVER WITH 2-6 GHz IF

Sarjit S. Bharj, S. P. Tan, J. Gluck, B. Thompson

ANADIGICS, INC.
35 Technology Drive
Warren, New Jersey 07060

ABSTRACT

A dual channel 2-20 GHz receiver with a 2-6 GHz IF has been designed and developed to give conversion gain and good LO and RF rejections at intermediate frequencies. It utilizes nine MMIC chips and has an 8 to 12 GHz MESFET voltage controlled oscillator. Applications of this receiver are intended for future electronic warfare systems. The receiver uses a unique planar balun for the double balanced mixer.

INTRODUCTION

A dual channel 2-20 GHz receiver with a 2-6 GHz IF has been designed and developed to give conversion gain and good LO and RF rejections at intermediate frequencies. The sub-system uses nine MMIC chips and a voltage controlled oscillator, tuneable over 8-12 GHz. The unit was designed for future electronic warfare applications and was intended to demonstrate the feasibility of using a large number of MMIC chips.

The subsystem block diagram is shown in Figure 1, which also shows chip partitioning. Each channel consists of a 2-18 GHz distributed amplifier, a 2-18 GHz passive in-phase power splitter, an MIC phase splitting network, a commutator mixer and a 2-6 GHz IF amplifier. Each channel is fed with an on-board local oscillator distribution network. This network provides 0° and 180° outputs that are necessary to drive the double balanced mixer. The design and development of the following are considered in detail herewith:

1. Distributed Amplifier
2. Phase Splitting Networks
3. Local Oscillator Distribution
4. Mixer and IF Amplifiers

The specifications for receiver are detailed briefly in Table I.

1. Distributed Amplifier

The distributed amplifier was implemented in the receiver channel in order to maintain a reasonable NF. The image noise for such a wideband system is not easily eliminated by use of bandpass filters, and a penalty of 3dB was considered to be acceptable.

This circuit is a two-stage distributed amplifier with on-chip bias network, fabricated on four mil GaAs substrate using substrate-via-hole and microstrip technology. Each stage is made up from four sections and each section is built around an active device which is a cascode of interdigital single gate FETs. The outermost of the four sections utilizes 200 micron single gate FETs, while the inner two sections contain FETs with 300 micron peripheries. The amplifier is shown in Figure 2.

The high impedance serpentine transmission lines, which dominate the layout, are primarily inductive in nature. The active device parasitics (Cgs, Cds, etc.) are primarily capacitive in nature. Combining these different reactances in this topology yields the series L - shunt C architecture of the familiar lumped element equivalent of a distributed transmission line. Actually, there are two of these "artificial" transmission lines, one involving the FET input parasitics and the other involving FET output parasitics. The parasitics of the active devices are, in essence, absorbed into these artificial transmission lines. The absorption of these parasitics leads to broader band performance. These two artificial lines are coupled to one another primarily through the transconductance of the FETs in the classic distributed amplifier arrangement. The amplifier has a measured 10 dB gain with a 2:1 VSWR to 18 GHz.

2. Phase Splitting Network

The network consists of an active 2-20 GHz in-phase power divider implemented in MMIC, the two outputs of which feed bandpass filter networks which have identical amplitude response, but are 180° out-of-phase. The filter network has been modified in a novel fashion to make it MMIC compatible. The active power splitter has compression points in the +15 dBm range and has an excellent phase tracking performance. The phase shifting filter networks have insertion loss in the region of 0.5 dB in mid-band.

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A block diagram of the network is shown in Reference [2]. It consists of an active power divider and two filter networks.

Wideband Active Power Splitter

The in-phase power divider is comprised of two single stage, four section, distributed amplifiers that share a single input transmission line structure. Identical distributed amplifiers are used in both arms. The excellent phase and amplitude performance obtained stems from this topological symmetry. The FET cell within each section is actually a cascode chosen to increase isolation. The cascode also extends bandwidth due to low drain line loading. Resistances in series with the second gate of each cascode provide stability. The schematic of the circuit and its performance are shown in Reference [2].

Phasing Circuit [1]

The basic building block for the wideband balun consists of a network of shorted coupled lines and a simple Pi network of transmission lines, as detailed in Reference [2].

The two networks are exactly equivalent for all frequencies except that the transmission phase difference between the two circuits is exactly 180° out of phase.

In order to obtain wideband performance, the shorted coupled line network was designed as a multisection Lange coupler. The dimensions of the coupler were obtained from an in-house program and optimized on Touchstone.

The filter networks were connected to the output of the divider. The measured performance is detailed in Reference [2].

The circuit provides excellent phase response from 2 GHz to 18 GHz. However, the amplitude response is good from 4 GHz to 18 GHz. Amplitude tracking was measured to be within $\pm$ 1 dB and phase to be within $\pm$ 7 degrees.

3. Local Oscillator Distribution Network

The local oscillator distribution network, consisting of an X-band voltage controlled oscillator feeding three active power dividers, has been developed. The function of the network is to provide four inputs to the local oscillator ports of the receiver channels. Each of the four outputs provides power output in excess of +8 dBm. In order to achieve the power output, active power dividers with zero dB loss have been used. Alternative methods would have required either a high power voltage controlled oscillator feeding passive Wilkinson divider or an oscillator followed by a power amplifier feeding a passive network. In the network described in this paper, the active power splitter has compression points in the +15 dBm range and has an excellent phase tracking performance. The X-band voltage tuned oscillator is capable of supplying in excess of 10 dBm power output and utilizes an off-chip hyperabrupt GaAs varactor. The phase splitters described earlier were also used for this network. The block diagram of the network is shown in Figure 3.

In the design of the oscillator, the value of the inductance between the gate and ground was selected to obtain a negative impedance when looking into the source of the active device. The drain was terminated in 50 ohms; negative impedance is such that, at resonance conditions, power is deliverable into a 50 ohm load. The negative impedance of the common gate configuration has an inductive reactance, and the value of the phase angle is controlled by the value of the inductance between the gate and ground.

For the oscillator to tune over X-Band, a phasing circuit was added to the source. The phase of this circuit is capacitance controlled using reverse bias voltage to the varactor diode. Figure 4 shows the performance of the local oscillator distribution network.

4. Mixer and IF Amplifier

The mixer circuit is comprised of three main sections, namely, two phase splitters or baluns providing equal amplitude antiphase signals for the signal and LO and a commutator circuit for performing the frequency conversion. A single gate GaAs FET was chosen for the active devices. Dual-gate FETs could have been used to implement this commutator, but our experience has shown that there is poor isolation between the gates, as low as 10 dB, when realized in the interdigital form.

The circuit that performs the frequency conversion process is the commutator. This circuit essentially comprises 2 RF amplifiers that are alternately switched into operation; ideally, only one functioning as an amplifier at any time. The alternate switching of these amplifiers is achieved by an LO signal at the gate of each FET, ideally, of equal magnitude and in antiphase (0° and 180°). When the antiphase LO signals are applied to the gates of two FETs, in series with the two devices acting as RF amplifiers, the two amplifiers are alternately turned on and off by the LO.

The signal balun is virtually identical in design to the LO balun. Although, at any instant in time, a signal appears at both outputs of the signal balun, only one is amplified via the commutator at any one time. The outputs from the two amplifiers in the commutator are combined in phase to form an IF signal. It can, therefore, be seen that, under ideal conditions, the output signal from the commutator will come first from the 0° output from the signal balun and, then, from the 180°

output. In this mixer design, the rate of commutation is determined by the LO. The mixer cell is shown in Figure 15, and consists of four half-micron MESFETs with a gate width of 200 microns. It operates from a single +5 volt supply, which is variable to give maximum conversion efficiency.

ANADIGICS' AWA 20601 amplifier was used as the IF amplifier following the mixer. The amplifier was therefore implemented as a macro cell and integrated with the mixer design.

Integrated Dual Channel Converter

A photograph of the assembled unit is shown in Figure 6. Each channel in this assembly was individually tested. The local oscillator frequency was set in two modes. In the first mode, the oscillator frequency was set from its tuning characteristics and, in the second mode, set by observing the local oscillator breakthrough at the IF output. The measurements were conducted by fixing the local oscillator frequency and varying the RF frequency to output IF frequency within 2 GHz to 6 GHz. RF frequencies were varied with the local oscillator, both above and below the RF frequencies. In addition, local oscillator and RF breakthrough levels were recorded. All the measurements were done at a signal level of -10 dBm.

Figure 7 shows the conversion loss data for Channel #1, with RF from 2 to 10 GHz. As shown, it has a conversion loss of 2 ± 2 dB over an IF bandwidth of 3 to 5.5 GHz. The data was measured with RF input of -20 dBm.

Figure 8 shows the conversion loss with RF from 10 GHz to 18 GHz. The conversion loss deteriorates at IF frequencies above 5 GHz. From 2 to 5 GHz, it can be specified as 0 ± 5 dB. For LO frequencies of 11 GHz and 12 GHz, the conversion loss is excessive. Figure 9 details the RF and LO rejection for Channel #1.

CONCLUSION

A wide band dual channel receiver was designed and developed successfully. The developent was a challenge.

REFERENCES

[1] Matthei, Young and Jones, Microwave Filters, Impedance Matching Networks and Coupling Structures, McGraw Hill, New York, pp. 219-230.

[2] S. Bharj et al," A 2 to 18 GHz 180 Degree Phase Splitter Network," MTT-1989.

PARAMETER	SPECIFICATION
RF Frequency	2 - 18 GHz
Noise Fig	14 dB
Conversion Gain	10 dB
RF to IF Isolation	< - 20 dB
Input Compression Level	0 dBm
Conversion Gain Flatness	< 2 dB over RF and IF Bands
Input VSWR	< 2.5:1
Supply Voltages	± 5 Volts
Phase Tracking	< 40 Deg.
Amplitude Tracking	< 3 dB
VCO Tuning Voltage	0 to -10 V
VCO Range	8 - 12 GHz
VCO Temp Stability	1 MHz/° C
Operating Temp Range	- 55° C to + 85° C
Mechanical Size	1" x 1" x .64"

Table I

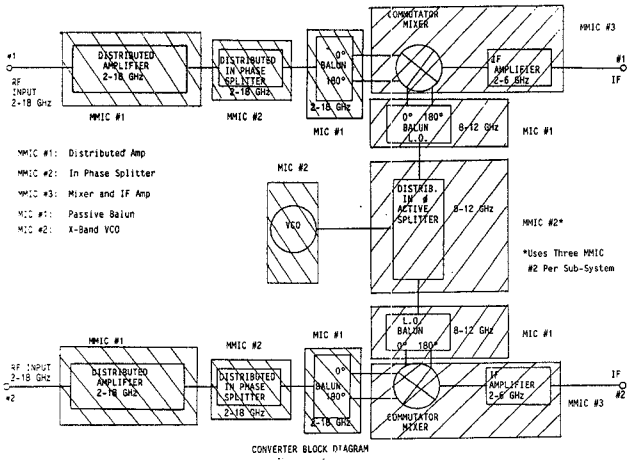


Figure 1

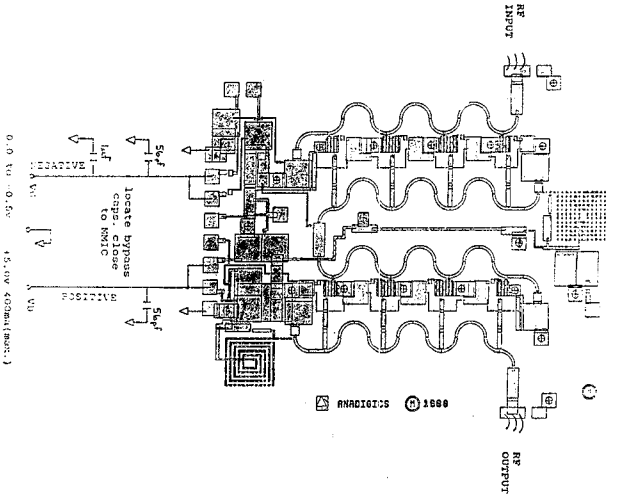


Figure 2

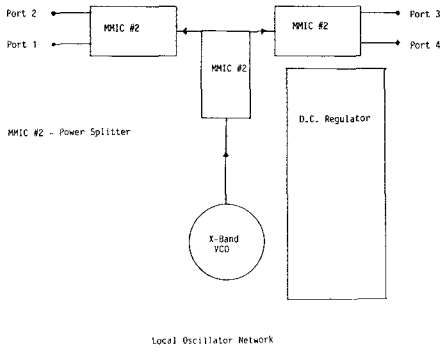


Figure 3

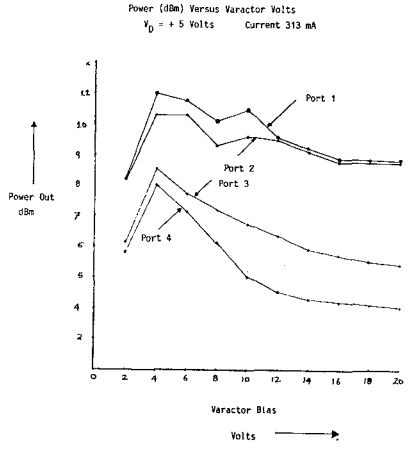
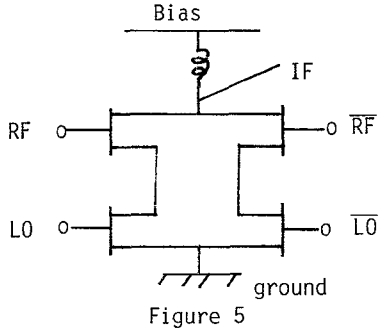


Figure 4



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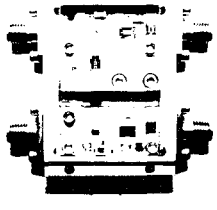

Figure 6

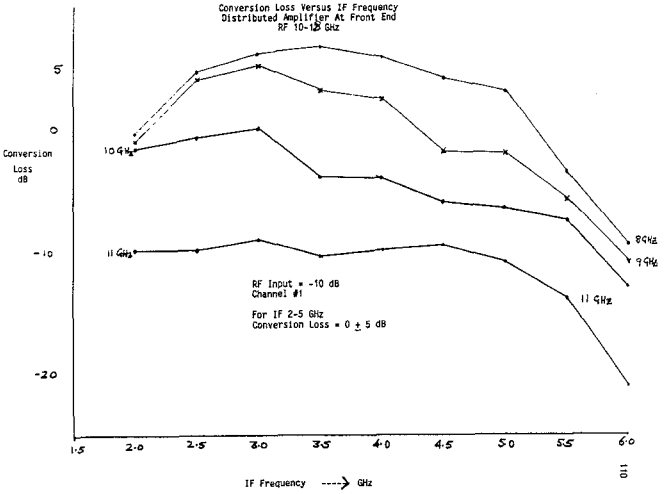

Figure 7

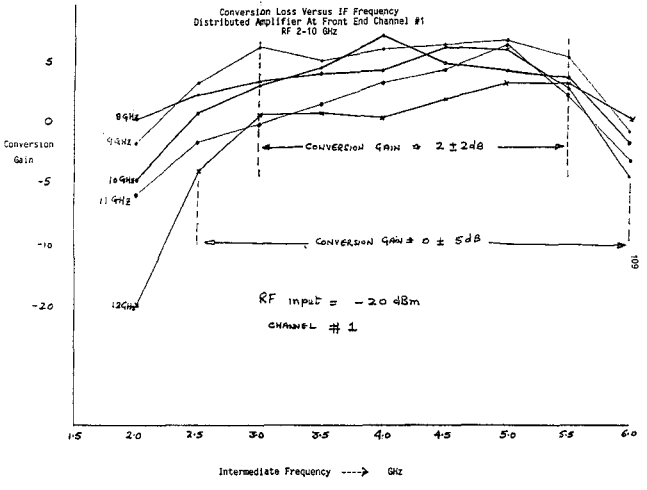

Figure 8

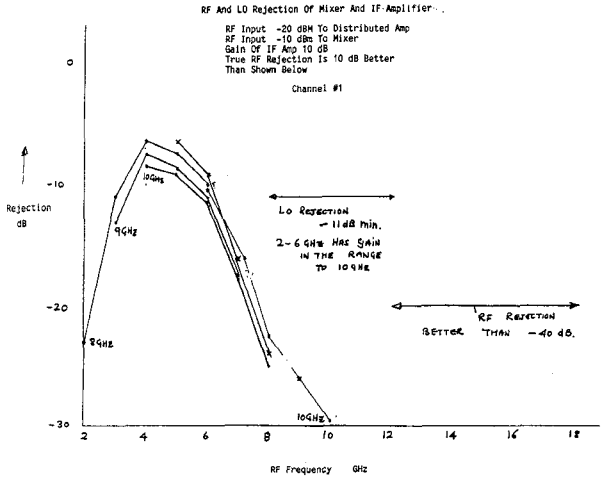

Figure 9